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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte N. JOHAN KNALL and MARK JOHNSON

Appeal 2009-009864
Application 10/689,187
Technology Center 2800

Before JOSEPH F. RUGGIERO, MAHSHID D. SAADAT,
and THOMAS S. HAHN, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1 and 2, which constitute all the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Introduction

Appellants' invention relates to a multi-level memory array having a plurality of memory cells wherein an insulating layer is used to form antifuses in the memory cells (*see* Abstract).

Exemplary independent claim 1 reads as follows:

> 1. A three dimensional multi-level memory array disposed above a substrate, the array comprising:
>
> a first plurality of spaced-apart rail-stacks disposed at a first height in a first direction above the substrate;
>
> a second plurality of spaced-apart rail-stacks disposed above the first height and in a second direction different from the first direction; and
>
> a plurality of memory cells, each memory cell comprising a silicon nitride antifuse,
>
> wherein the antifuses are disposed at the intersections of the first rail-stacks and the second rail-stacks.

The Examiner relies on the following prior art in rejecting the claims:

Mohsen	US 4,881,114	Nov. 14, 1989
Zhang (Zhang '396)	US 5,835,396	Nov. 10, 1998
Zhang (Zhang '302)	US 6,111,302	Aug. 29, 2000

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhang '396 and Zhang '302.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhang '396 and Mohsen.

The Examiner's Rejections

With respect to the obviousness rejection over Zhang '396 and Zhang '302, the Examiner relies on Zhang '396 for disclosing the recited three

dimensional multi-level memory array except for using silicon nitride as the metal-to-metal antifuse material for which the Examiner relies on Zhang '302 (Ans. 3-5).[1] The Examiner finds that the disclosure of silicon nitride or amorphous silicon as the antifuse material in Zhang '302 would have suggested to one of ordinary skill in the art to use silicon nitride, instead of amorphous silicon, as the antifuse material in the memory array of Zhang '396 (Ans. 4-5).[2]

Regarding the obviousness rejection over Zhang '396 and Mohsen, the Examiner again relies on Zhang '396 for disclosing the recited three dimensional multi-level memory array and on Mohsen for disclosing the claim 1 recited silicon nitride antifuse and the claim 2 recited doping levels of the polysilicon diodes (Ans. 5-8). The Examiner finds that the combination would have been obvious to the skilled artisan based on the known advantages obtained from using a silicon nitride antifuse (Ans. 6) and from including p^+n diodes to drive the memory cell (Ans. 7-8).

ISSUES

Has the Examiner erred in rejecting the claims as being obvious over Zhang '396 and Zhang '302 or over Zhang '396 and Mohsen because the proposed combinations do not teach or suggest using silicon nitride in metal-to-metal antifuses of Zhang '396, as recited in independent claim 1?

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[1] Throughout this opinion, we refer to the Answer mailed Dec. 31, 2008, the Appeal Brief filed Apr. 7, 2008, and the Reply Brief filed Feb. 16, 2009.
[2] The Examiner changed the initially stated position (Final Rej. 3) that using a silicon nitride antifuse would have been obvious in order to prevent "switch-off" to a position based on using a known antifuse material (Ans. 11).

FINDINGS OF FACT

The following Findings of Fact (FF) have support in the record by a preponderance of the evidence:

Zhang '396

1. Zhang '396 relates to read-only-memory (ROM) circuits, such as mask programmable ROM (MPROM) and electrically programmable ROM (EPROM), which are arranged in a two-dimensional array having a coupling mechanism at each cross-point of the matrix (col. 1, ll. 10-27).

2. As shown in Figure 4, a typical memory element comprises a ROM layer formed between top and bottom electrodes made of a metal or metal alloy where some examples include aluminum or copper (col. 5, ll. 15-22).

3. The ROM layer is referred to as MPROM layer in case of MPROM and as an antifuse layer in case of EPROM (col. 5, ll. 34-36, 47-49).

4. Figures 9A-9C show the EPROM structure having the metal layers 501 and 503 (similar to those shown in Figures 5A-5C made of aluminum or copper) and the antifuse layer 502*ca* made of amorphous silicon (col. 9, ll. 21- 29).

5. Figure 9B depicts another embodiment of the EPROM including the p-n diode 502*cb* and the antifuse layer 502ca wherein the p-n diode is similar to the diode shown in Figure 5C (col. 9, ll. 41-48) and is made of polycrystalline silicon (col. 6, ll. 50-54).

Zhang '302

6. Zhang '302 relates to conductor-to-conductor antifuses used in Field Programmable Gate Arrays (FPGAs) (col. 1, ll. 15-25) wherein the

problem of switch-off is solved by using low conductivity metals (col. 2, ll. 34-40).

7. The insulating antifuse layer is made of materials such as amorphous silicon, silicon nitride, silicon oxide, silicon oxi-nitride, or a combination thereof (col. 3, ll. 39-44).

Mohsen

8. Mohsen discloses a memory cell structure for Programmable Read Only Memory (PROM) including a dielectric layer formed between two electrically conducting layers having a high impedance before programming and a low resistance link and a PN diode after programming (*see* Fig. 1, col. 1, ll. 11-16; col. 2, ll. 44-51).

9. As shown in Figure 1, a moderately doped semiconductor material of a first conductivity type 12 and a heavily doped semiconductor material of a second conductivity type 16 form top and bottom electrodes, separated by the dielectric layer 14 (col. 3, ll. 47-55).

10. Mohsen further discloses that the dielectric layer 14 may be a silicon nitride layer (col. 4, ll. 22-24).

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' contentions that the Examiner has erred. We disagree with Appellants' conclusion (App. Br. 9; Reply Br. 4) that the combination is improper because the structures disclosed in the references are different and use different materials.

Rejection Over Zhang '396 and Zhang '302

With respect to specific materials and structures of the antifuse and metal contact layers, we note that the Examiner properly relies on Zhang '396 for disclosing the claimed three dimensional multi-level memory array where each memory cell includes an antifuse and on Zhang '302 for disclosing silicon nitride as the antifuse material (Ans. 3-5). While the specific conductor and antifuse materials disclosed in the references are different, we agree with the Examiner's findings (*see* Ans. 9-10) with respect to the memory cells in the references having similar basic operational principles. In that regard, we find that Zhang '396 discloses the recited memory cell array as the EPROM cells having antifuse layers between two conductor layers (FF 1-3).

We also agree with the Examiner's conclusion that based on the disclosure of Zhang '302, using silicon nitride as the antifuse material would have been obvious and available to the skilled artisan as one of the known antifuse materials. We understand Appellants' arguments to be focused on using low-thermal conductivity metal conductors and different materials for the quasi-conduction layer 502 in Zhang '396 (Reply Br. 4) and reasoning that the embodiments shown in Figures 5A-5C relate to an MPROM which include cells with no antifuse layer (Reply Br. 5-6). However, as found by the Examiner (Ans. 8-9), Zhang '396 describes the quasi-conduction layer 502 as the ROM layer which includes an antifuse layer in the EPROM structure shown in Figures 9A-9C (*see* FF 4-5). In other words, the EPROM of Zhang '396 also includes an array of memory cells, each including a metal-to-metal antifuse arrangement (FF 1-5). Additionally, Zhang '302 describes using low-thermal conductivity metal conductors to improve the

performance of a metal-to-metal antifuse structure of a memory cell including an antifuse layer formed of silicon nitride or amorphous silicon (FF 6-7). Therefore, the teaching value of Zhang '302 is the additional antifuse materials that are available to the skilled artisan. This is consistent with the decision by the Supreme Court, "the [obviousness] analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). "If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability." *Id.* at 417.

Rejection Over Zhang '396 and Mohsen

With respect to the Examiner's reliance on Mohsen for teaching a silicon nitride antifuse, Appellants present arguments similar to those asserted for Zhang '302, which we found unpersuasive. Appellants further contend that the combination is improper since Mohsen does not provide any advantages for using silicon nitride as the antifuse material (App. Br. 9-10; Reply Br. 7) and includes no p-n diode that existed before the antifuse is ruptured (App. Br. 10-11). We disagree.

Similar to our discussion above with respect to the combination of Zhang '396 and Zhang '302, we agree with the Examiner (Ans. 12) that Mohsen provides silicon nitride as a material for the antifuse structure of Zhang '396 which is known to the skilled artisan as an alternate material producing predictable results (FF 10). *See KSR*, 550 U.S. at 416. Additionally, as explained by the Examiner (Ans. 12-13), Zhang '396 discloses including the polysilicon p-n diode in the memory cell (FF 5),

whereas the specific doping levels could be determined by one of ordinary skill in the art based on the teachings of Mohsen (FF 8-9).

CONCLUSIONS

On the record before us, we conclude that, because the references teach or suggest all the claim limitations, the Examiner has not erred in rejecting the claims as being obvious over Zhang '396 and Zhang '302 or over Zhang '396 and Mohsen. Therefore, we sustain the 35 U.S.C. § 103 rejections of claims 1 and 2.

DECISION

The Examiner's decision rejecting claims 1 and 2 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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